REMARKS

The Examiner is thanked for the continued indication that claims 3 and 14 define allowable subject matter. The Office Action, however, has continued to reject all remaining claims. Applicant has made a sincere effort in this submission to place this application in condition for allowance. For example, although Applicants to not agree with the various rejections, Applicants have cancelled claims 20-24, to reduce the number of disputed issues.

Discussion of Rejections Under 35 U.S.C. § 112, First Paragraph

The Office Action rejected claims 20-24 under 35 U.S.C. § 112, first paragraph. These rejections have been rendered moot by the cancellation of these claims.

Discussion of Rejections Under 35 U.S.C. § 112, Second Paragraph

The Office Action rejected all claims under 35 U.S.C. § 112, second paragraph for various, stated reasons. In this regard, the Office Action noted phrases in claims 1 and 11, which rendered those claims unclear. Applicant has amended these claims to change the phrase "signal lines that comprise the system bus" to "signal lines that make up the system bus." Applicants respectfully submit that the corresponding rejections of claims 1 and 11 should now be withdrawn.

The Office Action also rejected claim 20 stating that the language of that claim is unclear. This rejection is rendered moot by the cancellation of claim 20.

Double Patenting Rejections

The Office Action rejected claims 1, 5-10, 11, 12, and 16-24 on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 6 and 8 of U.S. patent 7,343,440. This rejection appears inconsistent with the substantive rejections of independent claims 1 and 11, as allegedly being anticipated by U.S. patent 6,172,906 (hereafter the '906 patent). In this regard, the '906 patent was considered in the prosecution of the '440 patent, and the claims of the '440 patent were determined by Examiner Dang to patently define over the '906 patent. If independent claims 1 and 11 of the present application are so similar to claims of the '440 patent as to require a terminal disclaimer, it would seem that these claims would likewise patently define over the '906 patent.

Upon an indication of substantive allowability of the presently pending claims over the '906 patent, Applicant will submit a terminal disclaimer to overcome the double patenting rejections. It is premature to require the filing of a terminal disclaimer at this time, however, in view of the outstanding rejections.

Discussion of Rejections Under 35 U.S.C. § 102

On a substantive basis, the Office Action rejected the independent claims (claims 1, 11, and 20) under 35 U.S.C. § 102 as allegedly anticipated by the '906 patent. For at least the reasons set forth herein, Applicants respectfully request reconsideration of the rejections.

With regard to claim 1, claim 1 recites:

1. A single integrated circuit component comprising:

logic capable of being configured to interface with a first portion of a system bus, wherein the first portion of the system bus comprises only approximately half of a set of signal lines that make up the system bus; and

logic capable of being configured to interface with a companion integrated circuit, which companion integrated circuit is separate from the single integrated circuit component, and to receive information that is communicated from the companion integrated circuit, which information was communicated to the companion integrated circuit via a second portion of the system bus, wherein the second portion of the signal bus comprises a remaining portion of the system bus not included in the first portion, wherein the logic capable of being configured to interface with the first portion of the system bus is operatively connected with the logic capable of being configured to interface with the companion integrated circuit.

(*Emphasis added*). Applicants respectfully submit that claim 1 patently defines over the '906 patent for at least the reasons that the '906 patent fails to disclose the features emphasized above.

Notably, claim 1 (as amended herein) is directed to "A single integrated circuit component" (*i.e.*, a single component) that includes two separate logic blocks. A first logic block is capable of being configured to interface with a first portion of a system bus. Likewise, the second logic block is capable of being configured to interface with a companion integrated circuit **which is separate from the single integrated circuit component** and to receive information that is communicated from the companion integrated circuit, which information was communicated to the companion integrated circuit via a second portion of the system bus. Simply stated, these features are not disclosed in the '906 patent.

To assist the Examiner in a better understanding of claim 1, consider the embodiment of Fig. 2 of the present application. The integrated circuit corresponds to

reference numeral 210, while the companion integrated circuit corresponds to reference numeral 211. The first-recited logic element corresponds to split bus logic 214 of integrated circuit 210, while the second-recited logic element corresponds to split bus logic 215 of integrated circuit 210. As is illustrated in Fig. 2, and more particularly claimed in claim 1, the first-recited logic element (e.g., split bus logic 214) is capable of being configured to interface with a first portion of the system bus 105. Likewise, the second-recited logic (e.g., split bus logic 215) is configured to communicate and receive information that is communicated over a second portion of a system bus and routed through the companion integrated circuit 211. Similarly, claim 1 also covers the embodiment of Fig. 5.

As previously noted by Applicants, the teachings applied by the Office Action from the '906 patent (disclosing two memory chips 670 and 672 of a memory bank 506) are simply inapplicable to the embodiments defined by claim 1. In this regard, the two memory chips 670 and 672 of the '906 patent are separate integrated circuits, and not a single integrated circuit as required by claim 1.

On page 17 of the Office Action, the Examiner noted that the claims did not include the word "single." Applicants had believe this limitation was inherent in the preamble, which recited "An integrated circuit component" (meaning one component). However, as this omission appears to have been a significant factor in the rejection, Applicant has amended claim 1 to expressly define "A single integrated circuit component comprising." Simply stated, the '906 patent teaches just the opposite. As shown in FIG. 6A, relied on by the Examiner, reference numbers 670 and 672 designate different memory banks, which are in different semiconductor components. In this regard, col. 6, lines 60-62 of the '906 patent expressly states this, stating: "a first flash memory chip 670 designated FLASH0

and a second flash memory chip 672 designated FLASH1." The reference to these components as different "chips" implies that they are separate integrated circuit components, and not a single integrated circuit component, as expressly claimed in amended claim 1.

Further, and as discussed in Applicants' previous response, reference number 600 (of Fig. 6a) denotes a "memory system" (col. 6, line 36), and not a single integrated circuit. Reference number 506 denotes a "memory bank" (col. 6, line 57), and not a single integrated circuit. Finally, by the Examiner's own admission that reference number 670 comprises a first integrated circuit and reference number 672 comprises a second integrated circuit, the two separate integrated circuits cannot properly/logically comprise a single integrated circuit chip, as expressly claimed by claim 1.

In addition, lines 1-9 of col. 7 of the '906 patent actually state:

> Memory bus 512 includes a flash bus 675 connected to a port 676 of memory I/O unit 652 for transmitting address, data, and command signals between flash memory chips 670, 672 and the memory I/O unit 652. Flash bus 675 includes 16 bit lines, 8 bit lines of which form a first bus 680 connected to a port 682 of I/O register 671 of the first flash memory chip, and another 8 bit lines of which form a second bus 684 connected to a port 686 of I/O register 673 of the second flash memory chip.

Even accepting the interpretation of the '906 patent (as applied by the Office Action), the disclosure still fails to teach the claimed features. In this regard, assuming the sections 680 and 682 of the data bus comprises the claimed first and second plurality of signal lines, the memory chips 670 and 672 do not fulfill or provide the requisite features of claim 1. In this regard, claim 1 defines "***logic capable of being configured to interface with a companion integrated circuit*** **which is separate from the single integrated circuit component** ***and to receive information that is communicated from the companion***

integrated circuit, which information was communicated to the companion integrated circuit via a second portion of the system bus, wherein the second portion of the signal bus comprises a remaining portion of the system bus not included in the first portion, wherein the logic capable of being configured to interface with the first portion of the system bus is operatively connected with the logic capable of being configured to interface with the companion integrated circuit." No such comparable teaching or feature is disclosed in the'906 patent.

Simply stated, there is no teaching in the '906 patent of a single integrated circuit having logic for interfacing with a first portion of a system bus (the first portion being less than all of the system bus) and second logic for interfacing with a companion integrated circuit to receive information communicated over a second portion of the system bus. As claims 2-10 depend from claim 1, the substantive rejections of those claims should be withdrawn for at least the same reasons.

With regard to independent claim 11, claim 11 recites:

> 21. A system comprising:
> a plurality of separate, companion integrated circuit components that collectively implement a logic function embodied in a single, conventional integrated circuit component, ***each single companion integrated circuit component comprising***:
> a first logic interface for communicating with a remote component via ***a portion of a system bus, wherein the portion of the system bus comprises only approximately half of a set of signal lines that make up the system bus***;
> ***a second logic interface for communication with a companion logic interface of a remaining one of the plurality of the integrated circuit components over a separate bus, wherein the first logic interface is operatively connected with the second logic interface***; and
> logic for controlling the selective communication of information received by the first logic interface via the portion of the

system bus through the second logic interface to the companion integrated circuit.

(*Emphasis added*). Applicants respectfully submit that claim 11 defines over the '906 patent for at least the reasons that the '906 patent fails to teach those features emphasized above.

Like the rejection of claim 1, the Office Action cites memory chips 670 and 672 as comprising the claimed "integrated circuit." It then cites register 671 as comprising the claimed first logic interface. Then, the Office Action cites the same register 671 as comprising the claimed second logic interface. Applicant has explained above how the memory chips 670 and 672 cannot properly be interpreted as being part of the same single integrated circuit component. Like claim 1, Applicants have amended claim 11 to specifically define the integrate circuit component as being a "single" component.

As explained in Applicants' previous response, the first logic interface is specifically claimed as "communicating with a remote component via a portion of a system bus." In contrast, the second logic interface is specifically claimed as being configured for "communication with companion logic interfaces of the remaining of the plurality of the integrated circuit components over a separate bus." This is not taught or disclosed in the '906 patent. In fact, the only input to the applied I/O register 671 is bit positions D[0:7] of the data bus 680. These bit positions couple to I/O register 671 at reference number 682. Significantly, the register 671 cannot comprise the claimed second logic interface, assuming that that register 671 comprises the first logic interface. Furthermore, the I/O registers 671 and 673 are disposed in separate integrated circuit chips, so these elements cannot be mixed and matched as applying to the first and second logic interfaces, as claim

11 requires that the first and second logic interfaces be in a single integrated circuit component.

For at least these reasons, in addition to common reasons set out in connection with claim 1, the rejections of claim 11 should be withdrawn.

If the Examiner continues to disagree with these distinctions, Applicant respectfully requests that the Examiner more fully explain and reconcile these rejections based on the '906 patent with the double patenting rejections. As noted above, the '906 patent was considered in the prosecution of the '440 patent, and the claims of the '440 patent were determined by Examiner Dang to patently define over the '906 patent. If independent claims 1 and 11 of the present application are so similar to claims of the '440 patent as to be subject to a double patenting rejections, it would seem that these claims would likewise patently define over the '906 patent.

DUTY OF DISCLOSURE

With regard to the "duty of disclosure" issue that continues to be discussed by the Examiner, Applicants believe that this issue has been fully discussed in Applicants' previous response. However, as the Examiner continues to discuss the issue, the undersigned feels compelled to respond. In the present Office Action, the Examiner states:

> In response to Applicants' remark that "it was the undersigned or initially interviewed these applications with the inventors, it was the undersigned who drafted these applications, and it is the undersigned who has the best understanding of the relevant subject matter of these application, and the focus of their respective claims," it is irrelevant who has the best understanding of the relevant subject matter of these applications, and the

> focus of their respective claims. What is relevant here is whether the Applicants have filed multiple related applications without providing any information to this Office that these applications are closely related. What is important is whether Applicants have violated the requirement set forth by this Office, which clearly state that "no patent will be granted on an application in connection with which fraud on the Office was practiced or attempted or the duty of disclosure was violated through bad faith or intentional misconduct."

(*Emphasis in* original). In this regard, the Examiner continues to intimate that inequitable conduct has occurred. The undersigned disagrees.

First, the undersigned continues to disagree that this application and the issued U.S. patent 7,343,440 are the same. Indeed, the Examiner of this application is the primary Examiner who issued the '440 patent over the teachings of the Estakhri patent (the patent being used to substantively reject the claims of the present application). If the Estakhri patent, in fact, anticipates currently pending claims (as the Examiner has alleged), and since the Examiner admitted (through the issuance of the '440 patent) that the claims of the '440 patent patently defined over Estakhri, these facts are highly probative as evidence that the claims of the two applications are not directed to the same subject matter. Further, the Examiner seems to take the position that the subject matter of the two applications is the same because the two application share certain common figures. However, contradictory to this position, the Examiner (on page 12 of the present Office Action) states: "Applicants are also reminded that claimed subject matter not the specification, is the measure of the invention. Disclosure contained in the specification cannot be read into the claims…" Thus, on the one hand, the Examiner states that the proper focus of the "invention" is the claims. Yet, in the context of his "duty of disclosure" argument, the Examiner seems to ignore claim distinctions, and instead focuses on the certain common aspects of the two specifications. Simply stated,

the claims of the present application are patently distinct from the claims of the '440 patent, and as the Examiner has admitted, the proper focus when assessing the relevant "inventions" should be placed on the claims (not the specification, the inventors, or the filing dates).

Second, and more importantly, a conclusion of inequitable conduct requires a determination of both materiality and *intent*. Applicants accept that the Examiner disagrees with Applicants' position on materiality. However, with all due respect to the Examiner, the Examiner is simply in no position to make any conclusion with respect to Applicants' intent. Simply stated, at the time these applications were filed, the inventors considered the focus of the two applications to be patently different, and the undersigned attorney (having interviewed these disclosures and drafted the separate applications) agreed with this assessment. This assessment is consistent with the Examiner's different treatment of the claims of the two applications with respect to the Estakhri patent. There was not, and never has been, any intent to deceive the Examiner or the Patent Office in this or any relevant application. Consequently, no inequitable conduct has been committed.

CONCLUSION

In view of the foregoing, it is believed that all pending claims are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

No fees are believed to be due in connection with this amendment and response. If, however, any fees are deemed to be payable, you are hereby authorized to charge any such fees to Hewlett-Packard Company's deposit account No. 08-2025.

Respectfully submitted,

/Daniel R. McClure/

Daniel R. McClure
Registration No. 38,962

(770) 933-9500

Please continue to send all future correspondence to:

Hewlett-Packard Development Company, L.P.
Intellectual Property Administration
P.O. Box 272400
Fort Collins, Colorado 80527-2400